

25. An integrated circuit, comprising:  
a cache memory having a plurality of sets of cache frames for storing information  
from main memory; and

a cache allocation system for allocating one or more sets of said cache memory to  
one or more tasks.

26. The integrated circuit of claim 25, wherein one or more secondary tasks may use  
only said allocated sets of said cache memory and wherein one or more primary tasks may use  
unallocated sets of said cache memory.

27. The integrated circuit of claim 25, further comprising a mapper that transforms a  
set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set  
with said allocated portion of said cache memory.

28. The integrated circuit of claim 25, wherein said allocated sets of said cache  
memory can be varied by selecting an appropriate map function.

29. The integrated circuit of claim 25, further comprising a map register for  
identifying said one or more sets of said cache memory allocated to each task.

30. The integrated circuit of claim 25, wherein a desired location and size of said  
allocated sections of sets of said cache memory may be specified.